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EXAMINER
NGUYEN, LINH V

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 05/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	09/746,565	BOCK ET AL.	
	Examiner	Art Unit	
	Linh V Nguyen	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 July 2001* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claim 2 – 15, 17 – 32, 34 – 46, 48 – 51, and 53, are objected to because of the following informalities:

"A" beginning of each respective claim indicated above needs to replace with - - The - -.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1 – 52, are rejected under 35 U.S.C. 102(e) as being anticipated by Krymski et al. U.S. patent No. 6,476,751.

Regarding to claim 1, Fig. 7 Krymski et al. disclose an A/D converter, comprising: a plurality of capacitors and at least one comparator, arranged to form an analog to digital conversion of an analog input signal to a digital output signal; and a control circuit (Fig. 4)), controlling said capacitors to be used for both analog to digital conversion and for calibration.

Regarding to claim 2 wherein said control circuit controls a level, which is supplied to said capacitors (Fig. 4).

Regarding to claim 3, the converter further comprising a plurality of level latches, storing levels associated with calibration, and connected to control respective levels applied to said capacitors (LATCHES).

Regarding to claim 4, wherein said control circuit controls a level which is supplied to a bottom plate of each said capacitor, and wherein a top plate of each said capacitor is connected together to form a common line (Fig. 7).

Regarding to claim 5, the converter further comprising an image acquisition element, obtaining information indicative of a portion of an image, and producing an output indicative thereof, said an output being analog to digitally converted by said analog to digital converter (Fig. 5, 6, 7).

Regarding to claim 6 wherein said level supplied to a bottom plate of each said capacitors can be one of two different voltage levels or a ground level (Vdd or ground).

Regarding to claim 7, wherein said level applied to a bottom plate of each capacitor can be a first voltage level which is double a value of said first voltage level (no metes and bounds for this claimed invention because a first voltage level is a double value of said the first voltage level does not clearly defined the limitation of claimed invention).

Regarding to claim 8 wherein said image acquisition element is a MOS element (Fig.5, Col. 2 lines 33 – 35).

Regarding to claim 9, wherein said image acquisition element is one of a MOS photo diode or a MOS photo gate, and forms an active pixel sensor (Fig.5, Col. 2 lines 33 – 35).

Regarding to claim 10, wherein said control circuit includes a latch, latching a level, which is supplied to a bottom plate of each of a plurality of capacitors (Fig. 4, and Col. 2 lines 15 – 19).

Regarding to claim 11, wherein said level can be one of ground or one of two voltage levels (Vdd or ground see Fig. 7).

Regarding to claim 12, wherein said level can be one of ground or a single voltage level (Vdd or ground, see Fig. 7).

Regarding to claim 13, the converter further comprising a plurality of level latches, respectively storing levels associated with calibration, and connected to control a level applied to said capacitors (Fig. 4 and Fig. 7).

Regarding to claims 14 and 15, Although Krymski et al. does not explicitly disclose wherein said level latches store a negative version of a calibration level. And wherein said negative version is a two's compliment. However it has been held that a recitation with respect to the manner in which claim apparatus in intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claim structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).

Regarding to claim 16, Fig. 7 Krymski et al. disclose an A/D converter comprising: a plurality of capacitors, each associated with a specified bit of the digital signal, and each having a top plate connected to a common line and a bottom plate,

and a comparator, connected to receive said common line as an output of said capacitor at one input, and a signal at another input; and a plurality of value latches, each storing a value, and each associated with one of said plurality of capacitors, and changing a value applied to said bottom plate of said capacitor.

Regarding to claim 17, wherein said latches store either a one or a zero, and apply either a ground level or a reference level to said capacitor bottom plates depending on the value stored by said latches (inherently for digital values 1 or 0).

Regarding to claim 18, the converter further comprising a control circuit, controlling said value latches to store a calibration value, and use said calibration value during converting (Fig. 4).

Regarding to claim 19, wherein the same said capacitors are used both for calibration and for A/D conversion (Fig. 4, Fig. 7).

Regarding to claim 20, wherein said reference level includes two reference levels, one higher than the other (Col. 2 lines 61 – 63).

Regarding to claim 21, wherein said reference level includes a single reference level (Fig.5, Col. 2 lines 33 – 35).

Regarding to claim 22, the converter further comprising a switch, controlled by a level in said latch, and selectively providing either a ground level or a reference level to said capacitor (Fig. 7).

Regarding to claim 23, the converter further comprising an image sensing element, producing an output signal indicative of a portion of said image, said output

signal being coupled to said plurality of capacitors and comparator to be A/D converted thereby (Fig. 5 and Fig. 7).

Regarding to claim 24, wherein said image sensing element is an element formed in MOS (Fig.5, Col. 2 lines 33 – 35).

Regarding to claim 25, wherein said image sensing element is an active pixel sensor, having a photoreceptor, a follower associated with said photoreceptor, and a selector which allows electronic selection, also associated with said photoreceptor (Fig. 5, and see Col. 2 lines 48 – 57).

Regarding to claim 26, wherein said image sensing element is one of a photo diode or a photo gate (Fig.5, Col. 2 lines 33 – 35).

Regarding to claim 27, wherein said follower and said selector are each formed using CMOS (Fig.5, Col. 2 lines 33 – 35).

Regarding to claim 28, wherein said value latches are each formed using CMOS (Fig.5, Col. 2 lines 33 – 35).

Regarding to claim 29, wherein said value latches, said comparator and said capacitors, and a plurality of said image sensing elements, are each formed on a common substrate (Fig.5, Col. 2 lines 33 – 35).

Regarding to claim 30, wherein said value latches are formed of CMOS (Fig.5, Col. 2 lines 33 – 35).

Regarding to claim 31, wherein said value latches store a value calibration value (Fig. 4, and see Col. 2 lines 15 – 19).

Regarding to claim 32, although Krymski et al. does not explicitly disclose wherein said level latches store a negative version of a calibration level, and wherein said negative version is a two's compliment. However it has been held that a recitation with respect to the manner in which claim apparatus in intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claim structural limitations. Ex parte Masham, 2 USPQ2d 1647 (1987).33.

Regarding claims 33 – 51, Krymski et al. as applied to claims 1 – 32 above, disclose every aspect of applicant's method claimed invention.

Regarding to claim 52, Krymski et al. Fig. 5 disclosed An active pixel sensor, comprising: a semiconductor substrate (Fig.5, Col. 2 lines 33 – 35), having a plurality of items formed thereon, said items including: an image acquisition element (Fig. 5), formed using MOS formation technology, and having an MOS follower associated therewith and an MOS selection transistor associated therewith, said image acquisition element producing an output signal indicative thereof; and an A/D converter element also formed using MOS formation technology, including a plurality of capacitors and a comparator, said plurality of capacitors operating both to calibrate said A/D converter element and to convert signals applied to said A/D converter element, the same capacitors being used both for said calibrate and for said converter (Fig. 7), and further comprising a latch (Fig. 7 latches), having a plurality of digital storage portions, each formed of CMOS, and each storing a value based on said calibrate, said values used for allowing said A/D converter to acquire signals.

Regarding to claim 53, wherein said A/D converter is a successive approximation A/D converter (Col.1 line 16).

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh Van Nguyen whose telephone number is (703) 305-1934. The examiner can normally be reached from 8:30 – 5:00 Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Michael Tokar can be reached at (703) 305-3493. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

LVN

May 7, 2003

Michael J. Tokar

Michael Tokar
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